REMARKS

Allowable Subject Matter

Claim 21 has been amended as specified by the examiner.

'112 Rejection

The rejection of claim 20 under 35 USC 112 is respectfully traversed. The claim has been corrected.

'102 Rejection

The rejection of claims 1, 3 - 5, 8, 9, 19 and 22 is respectfully traversed.

The examiner has made a number of errors in reviewing the Sato reference.

Applicants call the examiner's attention to Figs 2G and 2H of Sato and the accompanying text on Col 5, lines 7 - 9, the preceding paragraph before the examiner's quoted selection, in which Sato states that CMP is used.

Applicants call the examiner's attention to Fig. 2F of Sato, showing that the isolation plug has a top surface below the top of the device layer, contrary to the examiner's statement in the bottom three lines of page 3 of the action and contrary to the requirements of claim 1.

In addition, claim 1 has been amended to specify that the fill in the isolation apertures has a height that is less than the the thickness (i.e. the top surface) of the pad insulator. Fig. 2G of Sato shows a fill in the isolation trenches that is clearly above the pad insulator 3.

Thus, the Sato reference is clearly not valid under 35 USC 102.

In addition, since the purpose of Sato's disclosure is filling a high aspect ratio trench, not the purpose of avoiding CMP, the disclosure is also not useful under 35 USC 103. One skilled in the art would not think to look at a disclosure that specifically calls for CMP to find a technique that avoids CMP, as claim 1 clearly specifies.

Independent Claim 19

With respect to claim 19, the foregoing remarks also apply. Applicants call the examiner's attention to Col 18, lines 52 - 55, which also state that CMP is used.

With respect to claim 22, Applicants call the examiner's attention to Fig. 12G, showing the result of a CMP treatment (col 18, lines 48 - 50). This embodiment is therefore not valid as a result of the restriction in all the independent claims that CMP is not used.

In addition, Applicants call the examiner's attention to Fig. 12H, showing that the isolation trench fill (numeral 8 in the Figure) is far above substrate 1 containing the device layer. Layer 15 is a polysilicon layer (col 18, line 6) that is patterned to form gates, not the device layer, which in conventional terminology contains the transistor body.

Claims 10 - 18 and 20

Claim 10 has been conformed to claim 1 and the remarks regarding claim 1 apply to claim 10 also.

In addition, the examiner has made another error on page 7, last three lines of the main paragraph: Fig2D of Sato does not show any field apertures, let alone those formed in areas disposed between apertures separated by greater than a minimum active area distance.

The label 'field aperture' has been defined in paragraph 35. Since it is merely a label applied to original text, there is no possibility of new matter being added.

Further, Chung shows the use of CMP (col 4, line 53).

Thus, the combination of Sato and Chung does not show the features of claim 10 or its dependent claims.

The examiner's assertions starting on page 8, in the paragraph starting "It would have been obvious" are merely assertions that the examiner has made up with no support in Sato or Chung.

Chung shows only a blanket implant, so that there is no support for finding the limitations of claims 11 and 12, directed at fully removing wide areas of pad insulator.

In summary, the combination suggested by the examiner comprises two references that each show the use of CMP. Applicants maintain that such a combination cannot possibly suggest a method that explicitly avoids the use of CMP.

For the foregoing reasons, allowance of the claims is respectfully solicited.

Respectfully submitted,

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